**LESSON PLAN**

**Subject Code & Name: Swing theory and Logic Design Branch: ECE**

**Class / Semester: II B.Tech I Semester Academic Year: 2016-17**

|  |  |  |  |  |  |
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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** |
|  |  | **Unit-1**  **Review of Number systems** |  |  |  |
| **1.** | **27.06.2016** | Number systems Base conversion methods | **1** | **CR** |  |
| **2.** | **28.06.2016** | Number systems Base conversion methods | **1** | **CR** |  |
| **3.** | **28.06.2016** | complements of numbers | **1** | **CR** |  |
| **4.** | **01.07.2016** | r’s, r-1’s compliment subtraction | **1** | **CR** |  |
| **5.** | **04.07.2016** | BCD | **1** | **CR** |  |
| **6.** | **05.07.2016** | Excess-3, Alphanumeric code | **1** | **CR** |  |
| **7.** | **05.07.2016** | self complement codes | **1** | **CR** |  |
| **8.** | **08.07.2016** | 2421 | **1** | **CR** |  |
| **9.** | **11.07.2016** | gray code | **1** | **CR** |  |
| **10.** | **12.07.2016** | error detection & correction codes, Parity checking codes, | **1** | **CR** |  |
| **11.** | **12.07.2016** | Hamming codes. | **1** | **CR** |  |
| **12.** | **18.07.2016** | Exam on unit 1 | **1** | **CR** |  |
|  |  | **Unit-2**  **Logic operations** |  |  |  |
| **13.** | **19.07.2016** | Logic Gates | **2** | **CR** |  |
| **14.** | **19.07.2016** | Boolean theorems | **2** | **CR** |  |
| **15.** | **22.07.2016** | Complements | **2** | **CR** |  |
| **16.** | **25.07.2016** | dual of logic expressions | **2** | **CR** |  |
| **17.** | **26.07.2016** | standard SOP | **2** | **CR** |  |
| **18.** | **26.07.2016** | standard POS | **2** | **CR** |  |
| **19.** | **29.07.2016** | Minimization of logic functions using theorems | **2** | **CR** |  |
| **20.** | **01.08.2016** | Multi level NAND – NAND,. | **2** | **CR** |  |
| **21.** | **02.08.2016** | Multi level NAND – NAND,. | **2** | **CR** |  |
| **22** | **02.08.2016** | NOR-NOR Realizations | **2** | **CR** |  |
|  |  | **Unit-3**  **Minimization of switching functions** |  |  |  |
| **23.** | **05.08.2016** | Minimization of switching functions using K-Map 2-variables | **3** | **CR** |  |
| **24.** | **08.08.2016** | Minimization of switching functions using K-Map 3-variables | **3** | **CR** |  |
| **25.** | **09.08.2016** | Minimization of switching functions using K-Map 4-variables | **3** | **CR** |  |
| **26.** | **09.08.2016** | Minimization of switching functions using K-Map 5-variables | **3** | **CR** |  |
| **27.** | **09.08.2016** | Minimization of switching functions using K-Map 5-variables | **3** | **CR** |  |
| **28.** | **12.08.2016** | code converters | **3** | **CR** |  |
| **29.** | **16.08.2016** | code converters | **3** | **CR** |  |
| **30.** | **16.08.2016** | binary multiplier using K-Map | **3** | **CR** |  |
| **31.** | **19.08.2016** | Tabular minimization | **3** | **CR** |  |
| **32.** | **26.08.2016** | Tabular minimization | **3** | **CR** |  |
|  |  | **Unit-4**  **Combinational logic circuits** |  |  |  |
| **33.** | **29.08.2016** | Design of Half adder, full adder | **4** | **CR** |  |
| **34.** | **30.08.2016** | half subtractor, full subtractor | **4** | **CR** |  |
| **35.** | **30.08.2016** | applications of full adders | **4** | **CR** |  |
| **36.** | **2.09.2016** | 4-bit binary adder, 4-bit binary subtractor, | **4** | **CR** |  |
| **37.** | **06.09.2016** | adder-subtractor circuit |  |  |  |
| **38.** | **06.09.2016** | BCD adder circuit, | **4** | **CR** |  |
| **39.** | **09.09.2016** | Excess3 adder circuit,. |  |  |  |
| **40.** | **13.09.2016** | look-a-head adder circuit | **4** | **CR** |  |
| **41.** | **13.09.2016** | Design of decoder | **4** | **CR** |  |
| **42.** | **16.09.2016** | Encoder | **4** | **CR** |  |
| **43.** | **16.09.2016** | Multiplexer | **4** | **CR** |  |
| **44.** | **19.09.2016** | Multiplexer | **4** | **CR** |  |
| **45.** | **20.09.2016** | Multiplexer |  |  |  |
| **46.** | **20.09.2016** | De-multiplexer | **4** | **CR** |  |
| **47.** | **26.09.2016** | Priority encoder | **4** | **CR** |  |
| **48.** | **27.09.2016** | Comparator | **4** | **CR** |  |
| **49.** | **27.09.2016** | Seven segment display | **4** | **CR** |  |
| **50.** | **30.09.2016** | Seven segment display |  |  |  |
|  |  | **Unit-5**  **Sequential logic circuits** |  |  |  |
| **51.** | **03.10.2016** | Classification of sequential circuits, | **5** | **CR** |  |
| **52.** | **04.10.2016** | Flip-flops with truth table | **5** | **CR** |  |
| **53.** | **04.10.2016** | Flip-flops with truth table | **5** | **CR** |  |
| **54.** | **07.10.2016** | Excitation tables | **5** | **CR** |  |
| **55.** | **17.10.2016** | Conversion of flip-flop to flip-flop. | **5** | **CR** |  |
| **56.** | **18.10.2016** | Design of ripple counters | **5** | **CR** |  |
| **57.** | **18.10.2016** | Design of ripple counters | **5** | **CR** |  |
| **58.** | **21.10.2016** | Synchronous counters | **5** | **CR** |  |
| **59.** | **24.10.2016** | Synchronous counters | **5** | **CR** |  |
| **60.** | **25.10.2016** | Johnson counters, ring counters. | **5** | **CR** |  |
| **61** | **25.10.2016** | Design of Buffer register, control buffer register, | **5** | **CR** |  |
| **62** | **28.10.2016** | Shift register,. | **5** | **CR** |  |
| **63** | **31.10.2016** | Bi-directional shift register | **5** | **CR** |  |
| **64** | **01.11.2016** | Universal shift register | **5** | **CR** |  |